In the Claims:

1. (CANCELLED)

2. (CURRENTLY AMENDED) ~~For use with an electronic~~ In an electronic signal processing apparatus containing a security key memory which stores a security key that enables a user to operate said electronic signal processing apparatus and a processor operatively connected to the security key memory, a method of preventing access to said security key in the event of a compromise in the integrity of a housing for said security key memory, said method comprising the steps of:

(a) monitoring the integrity of said housing; and

(b) in response to step (a) detecting said compromise in the integrity of said housing using the processor, changing the contents of said security key memory by using the processor to scramble the contents of the security key memory so as to effectively remove said security key from said security key memory, wherein

step (a) comprises storing, in a single-bit storage device, a single bit representative of a prescribed power supply state of said security key memory, and changing the bit state of said single-bit storage device in response to said compromise in the integrity of said housing for said memory such that the processor resets the single-bit memory device in response to an intrusion such that the security key must be rewritten into memory.

3. (PREVIOUSLY PRESENTED) The method according to claim 2, wherein step (b) comprises in response to step (a) detecting

a change in the bit state of said single-bit storage device, changing the contents of said security key memory so as to effectively remove said security key from said security key memory.

4. (PREVIOUSLY PRESENTED) The method according to claim 2, wherein step (a) comprises coupling a switch, having a closure state dependent upon the integrity of said housing, to said single-bit storage device, and in response to said compromise in the integrity of said housing, operating said switch, so as to change the bit state of said single-bit storage device.

5. (CURRENTLY AMENDED) ~~For use with an electronic~~ In an electronic signal processing apparatus containing a security key memory in which is stored a security key that enables a user to operate said electronic signal processing apparatus and a processor operatively connected to the security key memory, an arrangement ~~for preventing~~ configured to prevent access to said security key in the event of a compromise in the integrity of a housing for said security key memory, comprising:

a single-bit storage device which is coupled to the processor and coupled to store a single bit representative of a prescribed power supply state of said security key memory;

a switch, which is coupled to said single-bit storage device, and is ~~operative~~ configured to change the bit state thereof in response to said compromise in the integrity of said housing for said memory; and

~~a control circuit, which is operative,~~ wherein said processor is configured in response to said change in the bit

state of said single-bit storage device, to change the contents of said security key memory so as to effectively remove said security key from said security key memory by scrambling the contents of the security key memory and said processor resets the single-bit memory device in response to an intrusion such that the security key must be rewritten into memory

6. (CANCELLED)

7. (CURRENTLY AMENDED) In an electronic signal processing apparatus containing a security key memory, which stores a security key that enables a user to operate said electronic signal processing apparatus and a processor operatively connected to the security key memory, an arrangement ~~for preventing~~ configured to prevent access to said security key in the event of a compromise in the integrity of a housing for said security key memory, said arrangement comprising:

an intrusion detection circuit that is ~~adapted~~ configured to monitor the integrity of said housing; and

~~a memory contents modification circuit~~ a processor that is ~~operative,~~ configured in response to said intrusion detection circuit detecting a compromise in the integrity of said housing, to modify the contents of said security key memory and thereby effectively remove said security key from said security key memory by scrambling the contents of the security key memory, wherein

said intrusion detection circuit includes a single-bit storage device that is ~~operative~~ configured to store a single bit representative of a prescribed power supply state of

said security key memory, and a switch that is ~~operative~~ configured to change the bit state of said single-bit storage device in response to said compromise in the integrity of said housing for said memory wherein the processor resets the single-bit memory device in response to an intrusion such that the security key must be rewritten into memory.

8. (CURRENTLY AMENDED) The arrangement according to claim 7, wherein said memory contents modification circuit is ~~operative~~ configured, in response to a change in the bit state of said single-bit storage device, to change the contents of said security key memory so as to effectively remove said security key from said security key memory.

9. (ORIGINAL) The arrangement according to claim 8, wherein said switch has a closure state dependent upon the integrity of said housing.